

## A 2-Terminal Trapped Charge Memory Device With Voltage Switchable Multi-Level Resistance

Darrell Rinerson; Wayne Kinney; Steven W. Longcor; Edmond R. Ward; Steve Kuo-Ren Hsia; Christophe Chevallier

Contact: Morgan Malino of Beyer Weaver & Thomas, LLP, (650) 961-8300, Ref: UNTYP020

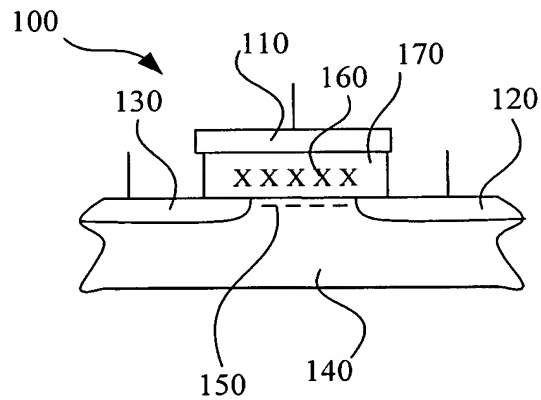


Figure 1 PRIOR ART

# A 2-Terminal Trapped Charge Memory Device With Voltage Switchable Multi-Level Resistance

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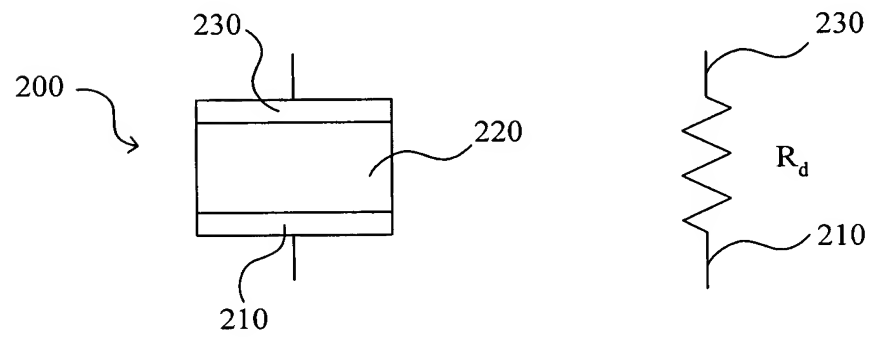


Figure 2

## A 2-Terminal Trapped Charge Memory Device With Voltage Switchable Multi-Level Resistance

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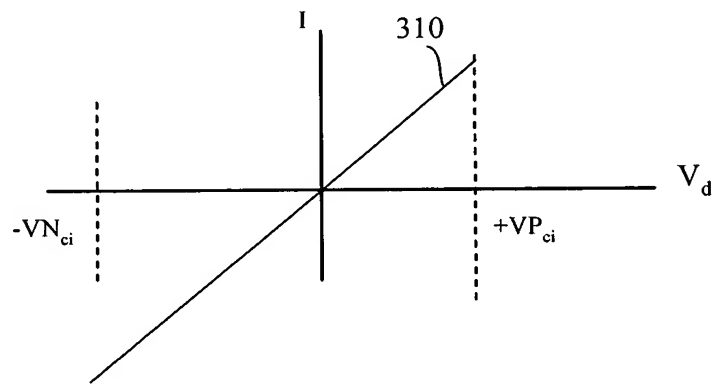


Figure 3A

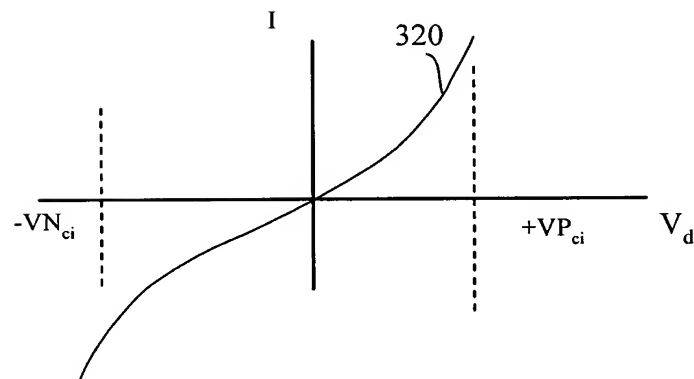


Figure 3B

## A 2-Terminal Trapped Charge Memory Device With Voltage Switchable Multi-Level Resistance

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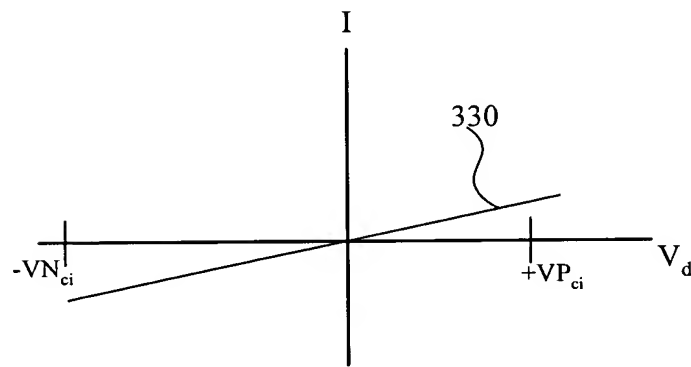


Figure 4

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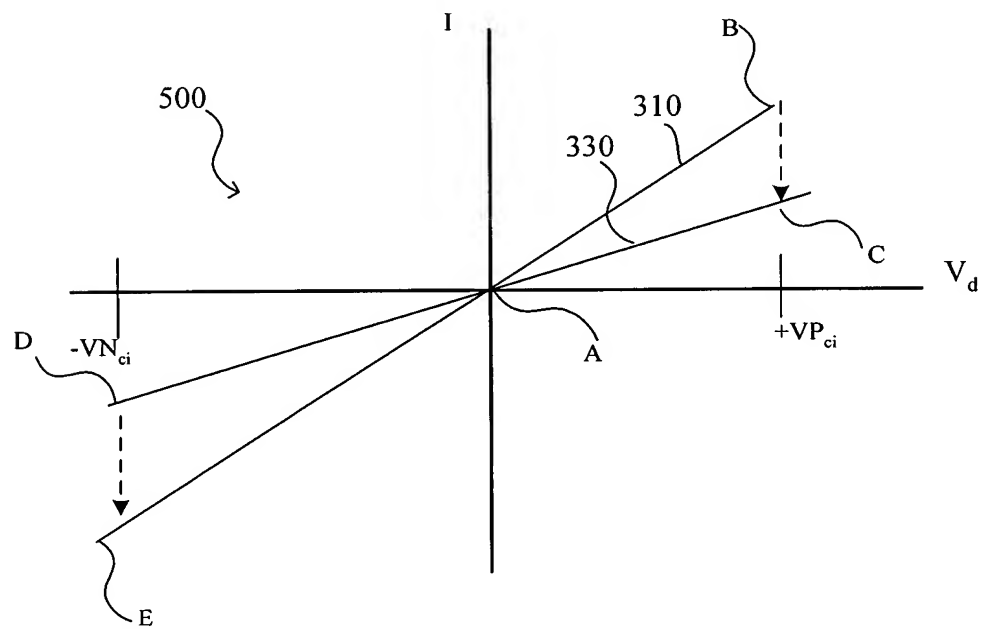


Figure 5

**A 2-Terminal Trapped Charge Memory Device With Voltage Switchable Multi-Level Resistance**

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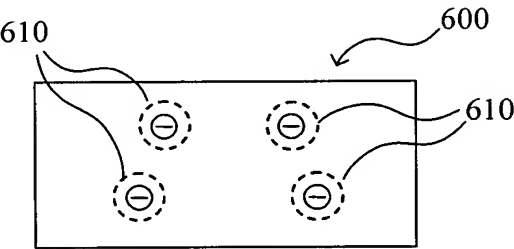


Figure 6A

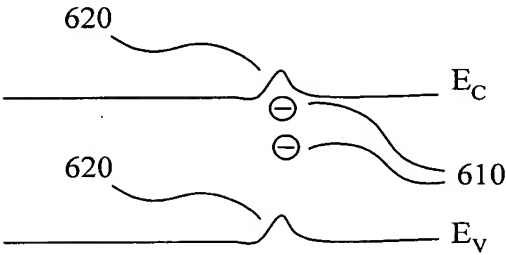


Figure 6B

## A 2-Terminal Trapped Charge Memory Device With Voltage Switchable Multi-Level Resistance

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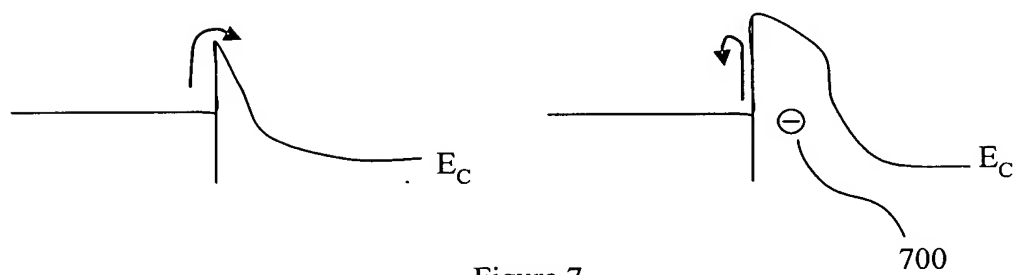


Figure 7

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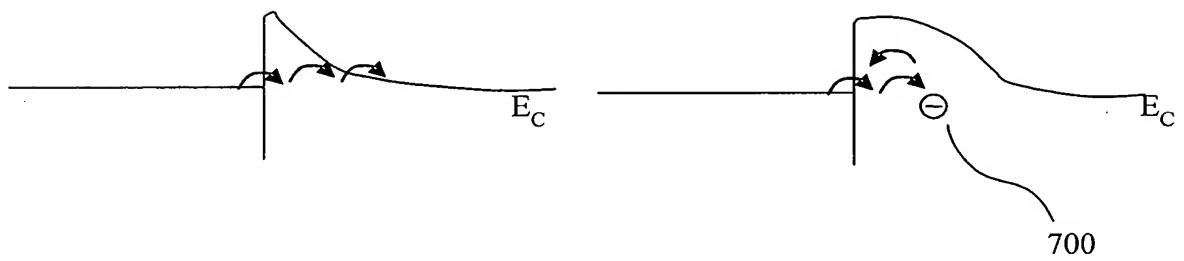


Figure 8



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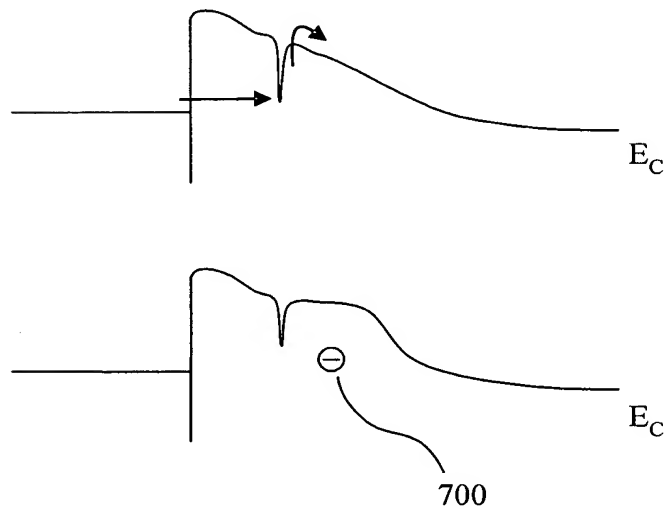


Figure 9

## A 2-Terminal Trapped Charge Memory Device With Voltage Switchable Multi-Level Resistance

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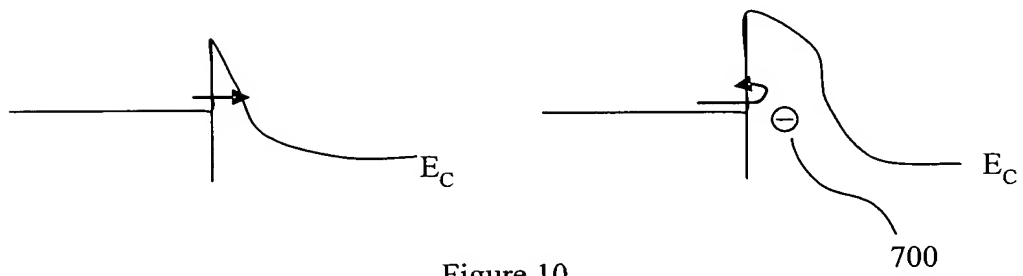


Figure 10